Focus 2

Innovation and Service

An Innovation Enabler
As the leader in dedicated IC foundry industry, TSMC has driven continued progress in global technology through innovation. We care about our customer’s feedback and have been expanding our R&D scale over the years. We insist on producing sustainable products with high quality and low energy consumption, and have also established a mechanism to protect our customer’s proprietary information. We hope to provide our customers next generation innovations and designs through leading technology and manufacturing excellence.

3,600 Patents/10,000 Trade Secrets
Protected intellectual property rights, with over 3,600 patents approved globally and over 10,000 trade secrets registered

93%
Maintained great working relationships, with customer satisfaction exceeding 90% for six consecutive years

>15 Billion (NT$)
Completed 49,356 quality improvement cases across departments, creating NT$15 billion in value
## Innovation Management

### Strategies & 2030 Goals

#### Technology Leadership
- Continuous investment and efforts on leading-edge technology development to maintain TSMC’s technology leadership in the semiconductor industry

#### Sustainable Products
- Assess the environmental and social impact of each stage in the entire product life cycle and provide our customers with products that have low environmental, carbon, and water footprints

#### Intellectual Property Protection
- Patent protection: continue to strengthen patent portfolio by keeping patent applications in sync with the Company’s R&D resources to make sure that all research achievements are fully protected
- Trade secret protection: enhance business operation and intellectual property innovation through trade secret registration and management that documents and consolidates the applications of the Company’s competitive trade secrets

### 2019 Achievements

<table>
<thead>
<tr>
<th>Technology Leadership</th>
<th>Sustainable Products</th>
<th>Intellectual Property Protection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Successful risk production of industry-leading 5nm process technology</td>
<td>Finished the product life cycle assessment on VisEra and TSMC fabs in Taiwan. Overseas subsidiaries are being built</td>
<td>Nearly 6,500 global patent applications</td>
</tr>
<tr>
<td>Target: Risk production of 5nm, the 5th generation FinFET CMOS platform technology for SoC</td>
<td>Target: Complete product life cycle assessment on all manufacturing fabs</td>
<td>Target: &gt;5,100 patents</td>
</tr>
<tr>
<td>5nm process technology in volume production</td>
<td>Complete the establishment of a digitalized internal environmental profit &amp; loss assessment system</td>
<td>Exceed 50,000 global patent granted</td>
</tr>
<tr>
<td></td>
<td>Complete environmental profit &amp; loss assessment on suppliers (including inventory on 50 key suppliers)</td>
<td>Exceed 100,000 trade secrets registered</td>
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### 2020 Targets

<table>
<thead>
<tr>
<th>Technology Leadership</th>
<th>Sustainable Products</th>
<th>Intellectual Property Protection</th>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Exceed 5,300 global patent applications</td>
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<tr>
<td></td>
<td></td>
<td>Exceed 12,000 trade secret registrations</td>
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</table>

Note: A Product Environmental Footprint regards environmental profit and loss as a comprehensive indicator.
Innovation Management Framework

In response to the rapidly evolving semiconductor industry, TSMC has been striving to build an innovative work environment that highly encourages innovation since its establishment. In the face of challenges imposed by existing and new competitors in 2019, TSMC continues to enhance the Company’s leading technological competitive advantages through an internal incentive scheme for innovation. Employees are encouraged to bring forth a variety of innovations to enhance organizational innovation vitality. Meanwhile, TSMC also dedicates resources to helping our customers, the industry, and academia drive interdisciplinary innovation collaborations, including product innovation with our customers, technical talent innovation with research institutions, and green innovation with our suppliers.

TSMC hosted an annual Idea Forum competition covering topics from Operations, R&D, Quality and Reliability, Corporate Planning Organization, and Finance, with suggestions from grassroots, Continual Improvement Team (CIT), Total Quality Excellence and Innovation Conference.

- Open Innovation Platform®
- Collaboration with World-class R&D Institutes
- TSMC University Programs
  - University Research Center
  - IC Layout Contest & Courses
  - University Shuttle Program
- University Programs
  - TSMC University Programs
- Open Innovation Platform®
- Collaboration with World-class R&D Institutes
- TSMC University Programs
- University Research Center
- IC Layout Contest & Courses
- University Shuttle Program

- Technology Leadership
- Intellectual Property Protection
- Intelligent Precision
- Manufacturing
- Innovation Cases
  - STOP & FIX Innovation
  - World Class Semiconductor Green Tools
  - The First Semiconductor Company to Receive AWS Certification
  - The First Company to Recover Fireflies
  - Major Waste Reductions in IPA
  - The Circular Economy “Three-Zero” Project
Technology Leadership

TSMC continued to expand its scale of research and development in 2019. The total R&D expenditure for the year was US$ 2.959 billion, a 4% increase from the previous year and 8.5% of the Company’s total revenue. The R&D team has grown to a team of 6,534 people, a 5% increase from the previous year. The scale of TSMC’s R&D investments is on par with top tech companies worldwide and even surpasses some of the company’s respectful counterparts.

Continuous Investment in R&D

To continue along the Moore’s Law trend and to assist our customers in successful, fast product development and delivery, TSMC has been continuously investing in R&D to offer industry-leading process technologies and design solutions. In 2019, following the transfer to manufacturing of the 7nm+ technology node and the successful risk production of 5nm technology, the Company’s R&D organization continued to fuel the pipeline of technological innovation needed to maintain industry leadership. While TSMC’s 3nm technology, the sixth generation of technology platform to make use of 3D transistors continues full development, the Company has initiated the development of 2nm technology, a pioneering effort within the semiconductor industry, and at the same time, is progressing in research and exploratory studies for nodes beyond 2nm.

In addition to developing CMOS logic technology, TSMC is also involved in the development of a wide range of other semiconductor technologies to satisfy customer’s demand for mobile SoC products and other applications, such as smartphones, high-performance computing, IoT, automotive electronics, etc.

Specialty Technologies / Integrated Interconnect & Packaging Technologies

- **3D IC and TSMC-SoIC® (System-on-Integrated Chips)**
  - Completed process validation for System on Integrated Chips (SoIC®), an innovative wafer-level package technology

- **Advanced Fan-Out and InFO (Integrated Fan-Out)**
  - Achieved high-volume production of Gen-4 Integrated Fan-Out Package on Package (InFO PoP) for mobile processor packaging
  - Successful qualification of Gen-5 InFO-PoP advanced packaging technology for mobile applications and Gen-2 Integrated Fan-Out on Substrate (InFO-oS) for HPC applications

- **Power IC/Bipolar-CMOS-DMOS (BCD)**
  - Developed 40nm BCD (Bipolar-CMOS-DMOS) technology – unique in the industry – offering leading-edge 20-24V HV devices with full compatibility to 40nm ultra-low-power platform and integration of RRAM, in turn, enabling low power, high integration and small footprint for high-speed communication interface in mobile applications

- **Embedded Flash Memory**
  - Developed 28nm eFlash for high performance mobile computing and high performance low-leakage platforms, which achieved technical qualification for automobile electronics and micro controller units (MCU)

- **CMOS Image Sensor Technology**
  - Developed the latest generation CMOS image sensors of sub-micron pixel for mobile applications and embedded 3D metal-insulator-metal (MIM) high-density capacitors for global shutter and high dynamic-range sensor applications

In 2019, TSMC maintained strong partnerships with world-class research institutions, including the Semiconductor Research Cooperation (SRC) in the U.S. and the Interuniversity Microelectronics Centre (IMEC) in the Belgium. TSMC also continued to expand research collaboration with leading universities throughout the world for two grand purposes; the advancement of semiconductor technologies and the nurturing of talent for the future.
Technology Leadership and Innovational Achievements

**Applications**
- 22nm ultra-low leakage (22ULL) technology began volume production to support IoT and wearable devices applications. In addition, 22ULL low-k/d low operating voltage solutions were ready.
- 36nm FinFET Compact RF (36FFC RF) technology delivered the world’s first FinFET device whose FT can reach >300GHz. This high-performance and cost-effective technology will be used in applications such as radar sensing and AR/VR to reduce chip power consumption and die size and to enable SoC designs.
- 22RF technology extended its support for 12-inch high voltage (HV) technologies, which demonstrated Organic light-emitting diode (OLED) devices. This technology can support various chip development for 5G mmWave mobile low leakage devices. This further supports wireless LAN power amplifier devices and ultra-small footprint for high-speed communication interface in mobile applications and delivered several customer products to market in high volume.
- Successfully supported customer to deliver 22nm ultra-low leakage devices. This further supports chip development for 5G mmWave mobile communication and IoT applications.
- 22ULL embedded RRAM technology started risk production. This technology can support various applications such as IoT MCUs and A memory devices.
- In work with customers, TSMC successfully demonstrated Organic light-emitting diode (OLED) on silicon panel technology on both 8-inch and 12-inch high voltage (HV) technologies, which paves the way for AR/VR suppliers to develop next generation goggles for various industrial, medical and consumer electronics applications.
- TSMC offers the next generation global shutter CMOS image sensor (GSS) and enhanced near infrared (NIR) CIS technologies, making machine vision systems safer, smaller, and consume less power.
- Successfully supported customer to deliver the world’s smallest CMOS-MEMS (micro-electromechanical systems) monolithic accelerometer in wafer level chip scale packaging (WL CSP) format, smaller than 1mm² in size. This small footprint can help reduce the size and weight of many IoT and wearable devices.
- Successfully developed InFO-PoP (Integrated Fan-Out Package-on-Package) technology which integrates 7nm SoC (System-on-Chip) and DRAM (dynamic random access memory) for advanced mobile device applications and delivered several customer products to market in high volume.
- Successfully developed InFO-PoP for 5G mmWave mobile communication and IoT applications.
- Developed the latest generation CMOS image sensors of sub-micron pixel for mobile applications and embedded 3D metal-insulator-metal (MIM) high-density capacitors for global shutter and high dynamic range sensor applications.

**2019**
- 7nm FinFET technology led the foundry to successfully entered risk production.
- 7nm FinFET plus technology entered customer volume production and led the world to deliver customer products to market in high volume.

**CMOS Logic Technologies**
- The World’s first 7nm automotive platform
- The one on the market with the highest level of performance in automotive applications
- Achieved High-volume production of Gen-4 Integrated Fan-Out Package on Package (InFO-PoP) for mobile processor packaging
- Successful qualification of Gen-5 InFO-PoP advanced packaging technology for mobile applications and Gen-2 Integrated Fan-Out on Substrate (InFO-sS) for HPC applications
- Developed 40nm BCD (Bipolar-CMOS-DMOS) technology - unique in the industry – offering leading-edge 24V HV devices with full compatibility to 40nm ultra-low-power platform and integration of RRAM, in turn, enabling low power, high integration and small footprint for high-speed communication interface in mobile applications
- Developed 28nm eFlash for high performance mobile computing and high performance low-leakage platforms, which achieved technical qualification for automobile electronics and micro controller units (MCU)
- Developed 16nm silicon in wafer level chip scale packaging (WL CSP) technology and delivered customer products to market in high volume for IoT and high-end smartphone applications.

**Specialty Technologies / Integrated Packaging Technologies for Conductors**
- Foundry’s first under panel optical fingerprint sensor technology in production
- Developed an industry’s unique 10nm BCD technology offering leading-edge 5-10V power devices and dense logic integration with competitive cost, as the next generation mobile Power Management IC (PMIC) solution.
- Mass production launch of new generation CMOS image sensors of sub-micron pixel for mobile applications and development of Ge-on-Si sensor for three dimensional range sensing applications with superior performance
- High-volume production of InFO PoP Gen-3 for mobile application processor packaging

**2018**
- N7+ technology entered risk production, the industry’s first commercially available EUV (extreme ultraviolet) process technology.
- Developed an industry’s unique 10nm BCD technology offering leading-edge 5-10V power devices and dense logic integration with competitive cost, as the next generation mobile Power Management IC (PMIC) solution.
- Mass production launch of new generation CMOS image sensors of sub-micron pixel for mobile applications and development of Ge-on-Si sensor for three dimensional range sensing applications with superior performance
- High-volume production of InFO PoP Gen-3 for mobile application processor packaging

**2017**
- N7 technology entered risk production, the industry’s first commercially available EUV (extreme ultraviolet) process technology.
- Completed the transfer to manufacturing of the industry leading 7nm technology, the fourth generation of technology to make use of 3D FinFET transistors.
- Launched the world’s leading volume production of 7nm FinFET technology for mobile applications and Gen-2 Integrated Fan-Out on Substrate (InFO-sS) for HPC applications
- Developed the latest generation CMOS image sensors of sub-micron pixel for mobile applications and embedded 3D metal-insulator-metal (MIM) high-density capacitors for global shutter and high dynamic range sensor applications.

**Technology Leadership and Innovational Achievements**
- The world’s leading volume production of 7nm FinFET technology for mobile applications and Gen-2 Integrated Fan-Out on Substrate (InFO-sS) for HPC applications
- Developed the latest generation CMOS image sensors of sub-micron pixel for mobile applications and embedded 3D metal-insulator-metal (MIM) high-density capacitors for global shutter and high dynamic range sensor applications.
Sustainable Products

When designing its product life cycle, TSMC factors in sustainability, hoping to reduce the environmental and social impact of its products. The Company puts efforts on assisting customers to achieve better energy efficiency throughout product design, material manufacturing, transportation, product manufacturing, testing, packaging, and other stages. In addition to its strong efforts in hazardous substance management, pollution prevention, and energy and resource conservation, TSMC also demands and assists its suppliers in thoroughly implementing environmental protection measures. The Company will continue to reduce the environmental, carbon, and water footprints throughout the life cycle of its semiconductor products.

Value Environmental Profit & Loss and Strive to Reduce Environmental Footprint

In 2019, TSMC finished the product life cycle, carbon footprint, and water footprint assessments on every manufacturing facility in Taiwan. The Company also achieved ISO14040, ISO14067, and ISO14046 certification. TSMC’s overseas subsidiaries are scheduled to be assessed and certified by a third party in 2021. According to the results of product life cycle, carbon footprint, and water footprint assessments, approximately 80% of the overall environmental impact derives from wafer fabrication. The secondary source of impact results from raw material production. The environmental impact of transportation is relatively mild. To learn more about TSMC’s efforts in reducing environmental impact, please refer to the “Green Manufacturing” section of this report.
In 2019, TSMC collaborated with Tunghai University on a research about each TSMC manufacturing fab’s energy and resources consumption, greenhouse gas emission, exhaust, wastewater, waste disposal, and other factors involved throughout the product life cycle. An assessment was conducted on the impact to external environment and human health, i.e., the environmental profit and loss (EP&L) assessment. Results show that the following factors, from most significant to least significant, have the greatest impact on the environment: greenhouse gas emissions (please refer to page 102 of this report), air pollutant emissions (primarily from ammonia), and effluent (primarily from heavy metals). TSMC has already implemented countermeasures to tackle ammonia emissions with early results yielding significant improvement; to learn more, please refer to the “Air Pollution Control” section of this report. As for the treatment of heavy metal in the effluent, in addition to continuing the existing practice of copper reduction and recycling, the company has newly established the cobalt recycling and treatment system in advanced manufacturing fabs in 2019. For more information, please refer to the "Water Management" section of this report.

Wafer Product Water Footprint Assessment
(eq average of an 8-inch wafer)

Wafer Product Carbon Footprint Assessment
(eq average of an 8-inch wafer)
Help Customers Create Energy-efficient & Sustainable Products

Through innovation and advanced manufacturing technology, TSMC continues to introduce more advanced energy-saving semiconductor products to enable ICT applications with better energy efficiency. In the meantime, TSMC is also extending applications of smart buildings, smart manufacturing, and smart grids. When global consumers or enterprises are continuously using a variety of products, which are produced on TSMC’s advanced semiconductor manufacturing process, the outstanding energy efficiency will significantly reduce global electricity consumption.

Since the aforementioned assumption requires further verification, TSMC will continue its collaboration with ISTI in researching about how semiconductor product applications that can contribute to energy conservation. The Company will further categorize its products in order to more precisely estimate TSMC’s contribution to energy conservation in Taiwan and worldwide.

More Advanced, More Capable, and More Energy-efficient Electronic Products

As the world’s most trusted dedicated foundry service provider, TSMC is consistently first to provide next-generation, leading-edge foundry technologies. The Company also offers comprehensive specialty technologies and excellent frontend and backend packaging integration capabilities. With TSMC’s manufacturing technologies, customers can unleash their design innovations in a wide range of applications including smartphone, high performance computing (HPC), Internet of Things (IoT), automotive, digital consumer electronics and so on. In light of the drastic change of global climate and the evolution of energy structure and technology development, chip products with stronger performance and higher power efficiency has become significant to electric product development. TSMC rigorously drives the semiconductor process technology development with higher density and reduced power consumption, which will provide customer with the leading advantages on performance, power, and area (PPA), helping customers produce more advanced, more capable, and more energy-saving products.

Semiconductor Applications Contribute to Global Energy Conservation

<table>
<thead>
<tr>
<th>TSMC’s Role</th>
<th>IC Products</th>
<th>Product Power Consumption</th>
<th>Impact on Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Leader of innovation and advanced process technologies</td>
<td>ICT products of better energy efficiency</td>
<td>Electricity consumption reduced by 0.197 trillion kWh (United States) Note</td>
<td></td>
</tr>
<tr>
<td>Provider of cutting-edge technologies</td>
<td>Extended applications of smart buildings, smart manufacturing, and smart grids</td>
<td>Electricity consumption reduced by 0.145 trillion kWh (Europe) Note</td>
<td></td>
</tr>
<tr>
<td>Producer of more advanced, energy-efficient products</td>
<td>Enhance energy efficiency of computers, communication networks, data centers, and power plants</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The adoption of end-electronic products like communications, data processing, and industrial products contribute to energy conservation on a national or regional level</td>
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</tbody>
</table>

Note: The results above are based on the assumption that TSMC’s technological development can have such impacts on global electricity consumption. The numbers are not the actual energy conservation figures contributed by TSMC.
One remarkable example is that Ambiq Micro delivered its Apollo3 Blue wireless SoC in 2019, setting a new standard in energy efficiency for battery-powered endpoint devices. Leveraging both Ambiq Micro’s Subthreshold Power Optimized Technology (SPOT™) platform and TSMC’s 40nm ultra low power (ULP) low operating power (low-Vdd) technology in TSMC’s IoT platform, the Apollo3 Blue with TurboSPOT™ brings groundbreaking levels of energy efficiency for battery-powered devices by increasing the computational capabilities of the ARM Cortex M4F core to 96MHz while lowering the active power consumption to less than six microamperes per megahertz (6uA/MHz). Apollo3 Blue’s unprecedented energy efficiency and superb computing power make it a key enabler for true intelligence to mobile, battery-powered endpoint devices, including IoT, hearable, wearable, and voice-activated products.

In total, TSMC deployed 272 distinct process technologies, and manufactured 10,761 products for 499 customers in 2019 to continue to bring significant contribution to the advancement of modern society.

TSMC Collaborates with Ambiq Micro to Unleash Innovation

- Provide 40ULP Low Vdd process technology
- Help Ambiq Micro deliver Apollo3 Blue wireless SoC
- ARM Cortex M4F core computational capabilities increased to 96MHz
- ARM Cortex M4F core active power consumption reduced to < 6uA/MHz
- Increase energy efficiency for IoT, hearable, wearable, and voice-activated products

Chip Die Size Cross-Technology Comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>Die Size (µm)</th>
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<tbody>
<tr>
<td>55nm</td>
<td>1.0</td>
</tr>
<tr>
<td>40nm</td>
<td>0.48</td>
</tr>
<tr>
<td>28nm</td>
<td>0.25</td>
</tr>
<tr>
<td>16FFC/12FFC</td>
<td>0.11</td>
</tr>
<tr>
<td>10nm</td>
<td>0.063</td>
</tr>
<tr>
<td>7nm</td>
<td>0.047</td>
</tr>
<tr>
<td>5nm</td>
<td>0.035</td>
</tr>
</tbody>
</table>

Note 1: The logic chip/SRAM/IO (Input/Output) ratio, which affects die size and power consumption, was re-aligned
Note 2: Source: TSMC

Die size is shrinking as line width shrinks

Chip Total Power Consumption Cross-Technology Comparison

<table>
<thead>
<tr>
<th>Technology</th>
<th>Power Consumption (µA/MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NSLP (1.2V)</td>
<td>1.0</td>
</tr>
<tr>
<td>N40LP (1.1V)</td>
<td>0.6</td>
</tr>
<tr>
<td>N28PM (0.9V)</td>
<td>0.3</td>
</tr>
<tr>
<td>N16FFC/12FFC (0.75V)</td>
<td>0.076</td>
</tr>
<tr>
<td>10nm (0.75V)</td>
<td>0.034</td>
</tr>
<tr>
<td>7nm (0.75V)</td>
<td>0.022</td>
</tr>
<tr>
<td>5nm (0.75V)</td>
<td>0.019</td>
</tr>
</tbody>
</table>

Note 1: The logic chip/SRAM/IO (Input/Output) ratio, which affects die size and power consumption, was re-aligned
Note 2: Source: TSMC

More power is saved as line width shrinks
Unleash Customer’s Innovations to Improve Human Health and Safety

Sensor makes all machines smarter, safer and more user and environmentally friendly. Optical, acoustic, motion, and environment sensors are mostly made with either CMOS image sensor (CIS) or micro-electromechanical systems (MEMS) technologies. TSMC continues to put substantial effort into developing new CIS and MEMS technologies to enable customers to innovate new products for new applications to bringing people a more convenient, healthy, and safe lifestyle.

- TSMC successfully supported customer to deliver the world’s smallest CMOS-MEMS monolithic accelerometer in chip scale packaging (CSP) format, smaller than 1mm² in size in 2019. This small footprint can help reduce the size and weight of many IoT and wearable devices.

Latest Achievements

- Extend CIS production applications from traditional RGB (red, green, blue) sensing to 3D depth sensing, optical fingerprint, and NIR machine vision, etc.
- Extend MEMS production applications from traditional motion sensing to microphone, bio-sensing, medical ultrasound actuators and more
- Adopted for consumer electronics, smartphones and other electronic devices to make life more convenient
- Adopted for advanced medical treatments and preventative health care applications to improve human health
- Adopted for automotive electronics to improve car safety systems

Unleash Customers’ Chip Innovations that Enhance Mobility and Convenience

7nm FinFET plus (N7+) technology entered volume production in 2019 and led to deliver customer products to market in high volume. N7+ technology is the world's first commercially available extreme ultraviolet (EUV) enabled foundry process technology. Its success demonstrates TSMC’s world-leading capabilities in EUV volume production.

- Innovative TSMC process technology helps chips achieve faster computing speeds in a smaller die area, leading to smaller form factors of electronic devices
- TSMC SoC technology integrates more functions into one chip, reducing the total number of chips in electronic devices, resulting in a smaller system form factor
- New TSMC process technology helps chips consume less energy so the mobile devices will have a longer battery life
- TSMC helps unleash more convenient wireless connectivity such as 3G / 4G and WLAN / Bluetooth, meaning people can communicate more efficiently and work anytime and anywhere, significantly improving the mobility of modern society
To ensure TSMC’s freedom in business operation, strengthen its industry leadership, and protect its leading-edge technologies which are the fruits of TSMC’s countless R&D efforts, the Company has set forth IP capitalization and management strategies in alignment with its business operation objectives and R&D resources. TSMC has also established a mechanism to generate company value from intellectual property. In addition, the Company continues to improve its IP portfolio quality, reduce maintenance costs, and invest in IP portfolio and IP management systems to assure the technology leadership and maximize business profits.

**Patent Protection Mechanism**

Internally, TSMC establishes a diversified reward system to encourage employees are encouraged to file patent applications for their inventions as diversity and innovation in design are highly valued and encouraged. The Company also has a systematic mechanism for patents and intellectual property set up a robust patent and IP management along system with a hierarchical review process to monitor the quantity and quality of employee patent applications. In 2019, TSMC held many Innovation-driven events for employees IP promotion activities including the Patent Campaign (with over 1,700 inventions submitted), Online Quiz Game (with nearly 3,500 participants), and Patent Week (with a 1,400-people turnout). These activities have successfully encouraged TSMC employees to file their inventions (493 employees received the U.S. patents for the first time at TSMC, contributing to a total of 375 patents. 8 prolific inventors contributed to 885 U.S. patents.)

Externally, TSMC has built close ties with both domestic and international patent offices through technical exchanges, assisting patent examiners in better understanding the technical content of TSMC and consequently accelerating the patent examination process in order to obtain high quality patent protection. In addition, TSMC has been assisting the government in building a sound and comprehensive intellectual property protection system by regularly sharing corporate experiences and suggestions on patent system and review efficiency.

**Four Strategies of IP Management**

TSMC’s IP management measures are implemented under four strategies, patent profiling, patent generation, patent portfolio expansion, and patent portfolio management. With its review mechanism, reward system, and education and training programs, the Company is dedicated to protecting its research and development results and upholding its industry-leading position.

**Achievements in Both Quantity and Quality**

- **Number of Patent Applications**
  - Over 55,000 global patent applications accumulated
  - Nearly 6,500 global patent applications filed in 2019
  - Top 10 patent applicant in the U.S. in 2019
  - No. 1 in Taiwan patent applications for four straight years

- **Number of Granted Patents**
  - Over 39,000 global patents accumulated
  - Received over 3,600 global patents issued in 2019, including over 2,300 U.S. patents

- **Patent Quality**
  - Highest patent approval rate, reaching 99%, among the top 100 patent holders in the US in 2019

For more details, please refer to TSMC CSR website: TSMC Creates a Global Strategic Patent Portfolio: Continue Pioneering in Top 10 of U.S. Patent Assignees for the Third Consecutive Year.
Trade Secret Protection

In order to comprehensively and effectively manage intellectual property innovation, TSMC records and integrates applications for trade secrets that contribute to the company’s technology leadership, manufacturing excellence, and customer trust.

In 2019, TSMC introduced advanced technology like Intelligent Automation (IA) and Artificial Intelligence (AI) into the Trade Secret Registration and Management System and continued to strengthen the company’s competitiveness. The system features prompt and effective data analysis and assistance for technology developers. In addition, the system is synchronized with other internal systems like human resources system and contract system to perform joint applications.

TSMC encourages its employees to keep trade secret in a centralized management system. In order to increase the quality and quantity of trade secrets, TSMC grants the annual Golden Trade Secret Awards to its employees to recognize their contribution. As of 2019, TSMC had given 1,335 awards to more than 4,600 employees who had registered trade secrets. In addition, the number of trade secrets registered has been increasing every year since the establishment of the Trade Secret Registration and Management System in 2013. As for 2019, over 10,000 trade secrets were registered, which set a new record in the Company’s history.

Intelligent Precision Manufacturing

As world’s largest semiconductor foundry service provider, manufacturing excellence is the cornerstone of TSMC’s competitive advantage. TSMC is the industry’s first automated manufacturer. Amid the increasing complexity of advanced manufacturing and customer demand on quality, TSMC has taken a further step to create an intelligent manufacturing environment featuring self-diagnosis and self-feedback capabilities. The Company has also applied AI to wafer fabrication and constructed a development platform with machine learning technology. Through constant Fab Alignment and benchmarking, TSMC has successfully reached a high level of consistency in quality throughout different fabs (Fab Matching), further strengthening the Company’s competitive advantages.

In 2019, dedicated to AI and knowledge integration, TSMC conducted industry-academia exchanges with Harvard University, University of Cincinnati, and the Ohio State University to introduce Industry 4.0 and Industrial AI to the semiconductor industry. Experts and engineers at the production line are called upon to jointly build a knowledge base for engineering analysis and to apply manufacturing experiences to AI intelligent models. It effectively improves the precision of intelligent models and allows for parameter adjustments in a dynamic manufacturing process. While securing wafer quality consistency, the Company also invests heavily in AI talent cultivation and acquisition. As of 2019, TSMC boasts a team of nearly 1,000 IT professionals and 200 experts on machine learning.

To fulfill its commitment to manufacturing excellence and quality, TSMC has enhanced the production capacity of 7nm advanced manufacturing process by 2% in 2019. The defect parts per million (DPPM) of automotive products was significantly reduced to 10 ppm in only three and a half years. With intelligent precision manufacturing, TSMC is able to continuously inject innovation vitality into the global IC industry and to be a trusted partner for customers to rely on for years to come.

For more details, please refer to TSMC CSR website: TSMC Adopts Intelligent Automation (IA) and Artificial Intelligence (AI) Technologies for Trade Secret Management Innovation
Manufacturing Excellence

- First automated 12-inch GIGAFAB® facilities in the industry built
- 100% automated wafer fabrication achieved
- Productivity of employees at mature manufacturing process foundries increased by 10% to 15% annually
- Wafer Big Data Infrastructure constructed
- Analysis results produced by artificial intelligence introduced to the manufacturing system
- Big Data Analytics for Semiconductor Manufacturing Contest held for three consecutive years in collaboration with MoST and NTHU, with 300 teams from 50 universities
- Big data courses collaborated and improved together with NTU, NTHU, and NCTU, providing both theoretical and practical teaching in class
- Machine learning development platform constructed to accelerate development and expand scale of application
- A program to cultivate 300 machine learning experts launched
- Research pool consisting of 1,000 IT experts and 300 machine learning experts built
- Efforts to develop advanced technologies and potential applications through the intelligent system continued
- Engage experts and professionals in the development of an AI model that integrates human knowledge and computer AI
- Conduct interdisciplinary exchanges with Harvard University, University of Cincinnati, and Ohio State University on the latest AI applications and development in semiconductor manufacturing

Cross-field Talent Development

- Scheduling and Dispatching
- People Productivity
- Equipment Productivity
- Process & Tool Control
- Quality Defense

Manufacturing Excellence
Open Innovation Platform®

TSMC’s Open Innovation Platform® promotes industry innovation for a comprehensive design infrastructure in the semiconductor design community by TSMC and its OIP alliance partners in EDA development, Intellectual Property (IP) implementation in order to achieve design & process technology co-optimization, also to provide backend packaging & test services and the enablement of IC designs in the Cloud.

In 2019, TSMC further teamed up with OIP alliance partners by combining EDA tool certification and OIP-VDE (Virtual Design Environment) in the Cloud, to ensure customers can more securely and efficiently work on their product design & innovation, thus shorten the design cycle and deliver to market faster to gain competitive advantages in business opportunities.

In 2019, TSMC and OIP ecosystem partners continue to provide comprehensive solutions to address the market demands for Mobile, HPC, Automotive and IoT design applications. Furthermore, there are continuous developments of new solutions to enhance Power, Performance and Area (PPA) on advanced & specialty process technologies, as well as comprehensive RF design platform for emerging markets, such as 5G design applications. The wide range of 3DIC ecosystem that covers both technology & application aspects is aimed to unleash customer’s innovation to efficiently design and successfully roll out more sophisticated high quality products.

In addition to industry collaborations, TSMC also provides long-term support to universities around the world, including National Taiwan University, National Chiao Tung University and National Tsing Hua University, helping them to conduct silicon validation of their research through TSMC University Shuttle Program.

Through the collaboration within OIP VDE from Cloud Alliance, TSMC and the University of Tokyo announced an alliance in 2019 that TSMC will provide its CyberShuttle® service to the Systems Design Lab at the University of Tokyo to jointly research semiconductor technologies for the future of computing.

In 2019, TSMC and Arm, the High Performance Computing (HPC) industry leaders, announced an industry-first 7nm silicon-proven chiplet system leveraging TSMC’s Chip-on-Wafer-on-Substrate (CoWoS®) advanced packaging solution. This establishes a robust foundation for future production-ready infrastructure of System on Chip (SoC) solutions.

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TSMC’s Five OIP Alliances

- **EDA Alliance**
  - The foundry segment’s earliest and most comprehensive Electronic Design Automation (EDA) certification program, delivering timely design tool enhancement required by new process technologies

- **Value Chain Aggregator Alliance**
  - Integrate design enablement building blocks and provide specific services at each link in the IC value chain, including IP development, backend design, wafer manufacturing, assembly, and testing

- **IP Alliance**
  - The foundry segment’s largest, most comprehensive and robust silicon-proven Intellectual Properties (IP) portfolio

- **Cloud Alliance**
  - Offering OIP Virtual Design Environment (OIP VDE), lowering entry barriers of Cloud adoption for the customers of all sizes to speed up silicon design in a big way by fully utilizing the high performance compute available in the Cloud

- **Design Center Alliance**
  - Offering services ranging from system-level front-end design to back-end physical/test implementation
OIP Objectives

By

- Collaborating with EDA and IP partners to
- Embed TSMC silicon technology into their products and services

Help Customers

- Access TSMC technology earlier in the design cycle
- Increase correlation between EDA tools and TSMC silicon
- Attain optimum PPA (Power, Performance, Area) in TSMC and third party IPs targeted for TSMC silicon

Advanced Technology

- In 7nm, 6nm, 5nm and smaller process nodes

Specialty Technology

- In Ultra-Low Power (ULP), Ultra-Low Leakage (ULL), RF, Analog, Bipolar-CMOS-DMOS (BCD), Non-Volatile Memory (NVM), High Voltage (HV), Sensor, etc

3D IC Technology

- Offering System on Integrated Chips (SoIC), Wafer on Wafer (WoW), Integrated FanOut (InFO), Chip on Wafer on Substrate (CoWoS), etc
TSMC University Programs

**University Research Center**

TSMC has established research centers in collaboration with top universities in Taiwan and dedicated research funds to encourage university professors to conduct groundbreaking semiconductor research projects. As the research centers strive to develop leading-edge technologies in semiconductor devices, material science, manufacturing process, and IC design, they are also incubating talents for the field of semiconductors. Up to 2019, more than 178 professors and 2,500 outstanding students in areas including electronic engineering, physics, material science, chemistry, chemical engineering, and mechanical engineering joined TSMC’s university research centers. Moreover, TSMC has also launched “TSMC Semiconductor Program” for the first time in 2019, and attracted over 200 students to enroll. Jointly developed by TSMC and the university, the courses are tailored to narrow the gap between industries and academics, and strengthen talent quality as well as competitiveness in the industry. TSMC will also continue to work with other universities to develop comprehensive semiconductor programs on device/integration, process/module, and equipment engineering.

In addition to investing in university research centers, TSMC also conducts strategic research projects with universities in Taiwan and overseas through industry-academia joint development projects. A variety of innovative research topics cover technologies in transistors, conductors, photomasks, materials, simulations, and special processes. In 2019, TSMC has collaborated with 7 universities in Taiwan and 15 universities overseas. 73 professors were involved in a total of 79 joint development projects with TSMC, with annual research funds exceeding NT$113 million. As of 2019, more than 100 U.S. patent applications had been filed.

University Research Center & Industry-Academia Joint Development Project

<table>
<thead>
<tr>
<th>Collaboration Project</th>
<th>University</th>
<th>Beneficiary</th>
<th>Collaboration Details</th>
<th>Dedicated Resources</th>
</tr>
</thead>
<tbody>
<tr>
<td>University Research Center</td>
<td>National Chiao Tung University, National Taiwan University, National Cheng Kung University, National Tsing Hua University</td>
<td>Undergraduate students, Graduate students, PhD students</td>
<td>Provide research assistantship to encourage outstanding students to focus on the study of semiconductor devices, materials, manufacturing processes, and IC design without financial issues</td>
<td>Total of NT$15.36 million research assistantship granted in 2019...</td>
</tr>
<tr>
<td>Industry-Academia Joint Development Project</td>
<td>7 universities in Taiwan and 15 universities overseas</td>
<td>Professors</td>
<td>Offer research funds to encourage university professors to propose new semiconductor research programs and incubate semiconductor talents</td>
<td>NT$111.3 million</td>
</tr>
</tbody>
</table>

Note: Maximum amount granted to undergraduate program is NT$100,000, NT$120,000 to a graduate program, and NT$360,000 to a PhD program. Scholarship was granted to 78 undergraduate students, 20 graduate students, and 51 PhD students in 2019.

7 Universities in Taiwan
National Chiao Tung University, National Taiwan University, National Cheng Kung University, National Tsing Hua University, National Sun Yat-sen University, National Taiwan University of Science and Technology, and Chang Gung University

15 Overseas Universities
Massachusetts Institute of Technology, Stanford University, University of California, San Diego, Georgia Institute of Technology, Harvard University, University of Michigan, University of Wisconsin-Madison, University of California, Berkeley, University of Illinois at Urbana-Champaign, University of Texas at Dallas, Cambridge University, Tyndall National Institute, Ireland, The Chinese University of Hong Kong, and Tohoku University
Launch Semiconductor Programs in Collaboration with Top Universities to Incubate Semiconductor Talent

To foster a vibrant environment for semiconductor talents in Taiwan and further attract more outstanding students to join the semiconductor industry, TSMC launched “TSMC-NTHU” Semiconductor Program in collaboration with National Tsing Hua University in 2019. More than 200 students enrolled in the elective courses. TSMC Semiconductor Programs in collaboration with National Taiwan University, National Cheng Kung University, National Taiwan University of Science and Technology, and National Taipei University of Science and Technology are scheduled to open for student enrollment in 2020.

First Program in 2019 Offers Outstanding Students with Internships, Job Interviews & Better Compensation

The TSMC Semiconductor Program is designed to enhance the professional competencies required for talents in the field of advanced process research and development. Programs are developed on two major tracks, “device/integration” and “processing/module,” and offers 24 courses covering next-generation device development, advanced process integration technology, material analysis technology, and more.

In addition to launching course on campus, TSMC also offers prioritized internship opportunities and guaranteed interviews for full-time job openings in the Company to students who have completed the program. Differentiated compensation package is also offered as an incentive to join TSMC. The program is an effort to not only incubate more talent in the field of advanced process research and development for semiconductor industry, but also to set an example for more companies to follow. It is hoped that with this cooperation, the gap between industry and academics could be minimized and domestic talent’s quality and competitiveness to be enhanced for the industry.

For more details, please refer to TSMC CSR website: TSMC and Top Universities Jointly Launch Semiconductor Programs to Incubate Semiconductor Talents

Sinn-Wen Chen
Senior Vice President, National Tsing Hua University

TSMC’s programs are like the guideline for dummies. Students with no ideas about their own future won’t get lost along the path of the programs.

Cheng-Yuan Chiu
Student of the Department of Engineering and System Science, National Tsing Hua University

TSMC-NTHU Semiconductor Program Course Plan

<table>
<thead>
<tr>
<th>Device Next-Generation Device Development</th>
<th>Processing Advanced Processing and Integration Technology</th>
<th>Material Failure Analysis of Integrated Circuits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advanced Device Development</td>
<td>IC Technology</td>
<td>Material Analysis Technology</td>
</tr>
<tr>
<td>2. Introduction to Solid-State Physics</td>
<td>2. Electronics 1</td>
<td>2. Applications of Synchrotron X-ray Absorption Spectroscopy</td>
</tr>
<tr>
<td>5. Measurements of Device</td>
<td>5. Applied Photonics</td>
<td></td>
</tr>
<tr>
<td>7. Engineering Mathematics 1</td>
<td>7. Electronic Thin Film</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10. Experimental Design and Statistics Applications</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11. Special Topic on Advanced Process and Integration</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12. Semiconductor Experiment</td>
<td></td>
</tr>
</tbody>
</table>

For more details, please refer to TSMC CSR website: TSMC and Top Universities Jointly Launch Semiconductor Programs to Incubate Semiconductor Talents
IC Layout Contest & Courses

Technology evolves rapidly. To continue along the Moore’s Law trend, TSMC has been driving semiconductor nodes towards 7nm process technology and further. In light of increasingly intricate advanced process technologies, the quality of chip layout affects overall performance by as much as 20%. TSMC sets out to provide our customers with competitive advantages of power, performance, and area (PPA) on TSMC’s advanced processes to win market opportunities. To fulfill our commitment, we are leading the industry in the cultivation of top IC layout talents well-versed in design and technology co-optimization (DTCO).

In 2019, TSMC launched the first national IC Layout Contest to further enhance the learning effects of “TSMC-NTUT IC Layout and Design,” a program that has been running for four years to prepare students for the future with industry links and experiences. To fulfill our commitment, we are leading the industry in the cultivation of top IC layout talents well-versed in design and technology co-optimization (DTCO).

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TSMC IC Layout Contest

- Preliminary Cross-Campus Campaign
  - 15 technical seminars held across Taiwan to help students learn more deeply about the opportunities and challenges of IC layout in advanced technologies
  - 2,000 students participated in the seminars
  - A total of 1,000 students and 150 advising professors from 35 universities in Taiwan signed up for the contest

- Contestant Training
  - 7 hours of advanced IC layout skill and electronic design automation (EDA) software online course co-developed with Microsoft Azure and Cadence
  - 12 weeks of free access to cloud-based Virtual Design Environment (VDE) for hands-on practices
  - 3 workshops where contestants learn directly from TSMC layout engineering experts
  - 8 hours of advanced training for finalists conducted by TSMC layout engineering experts, offering tips and explaining test questions in the preliminary round

- Outcome
  - Preliminary Contest
    A total of 250 teams, 500 students\textsuperscript{Note 1} participated in the contest
  - Finals
    17 teams, 34 students made it to the finals
  - Prizes
    Awarded with cash prize\textsuperscript{Note 2} and priority status for selection to TSMC summer internship opportunities

Note 1: The contest was originally designed with 300 contestants. Due to an overwhelming influx of entries, the limit was adjusted to 500, and lots were drawn to confirm official contestants out of 1,000 applicants.

Note 2: The first place, second place, third place, and honorable mention teams won NT$200,000, NT$100,000, NT$80,000 and NT$20,000 prizes and plaques, respectively. Additional plaques and a NT$10,000 cash prize were given as completion awards to all the teams who persisted in completing the competition.

IC Layout Courses

- Course Title: TSMC-NTUT IC Layout and Design Courses
  - 18 lessons in one semester
  - National Taipei University of Technology (NTUT): Theories and teachings
  - TSMC: Lecturers designated by TSMC Layout Design Engineering Division to demonstrate circuit layout design with case studies
    - Provide key IC manufacturing process, layout techniques and IP resources
    - Onsite instruction and Q&A
    - Offer summer internship opportunities
  - Frequency: Once a year
  - Number of Beneficiaries: A total of 120 students since 2016

Min-Yang Chiu
Contestant/ graduate student, Department of Electrical Engineering, National Tsing Hua University

For more details, please refer to TSMC CSR website: TSMC Leads the Industry by Hosting the First “TSMC IC Layout Contest” in the Cloud
TSMC University Shuttle Program

In 2019, TSMC University Shuttle Program helped professors and students of 25 universities around the world in turning IC design into actual chips and verifying the application performance of their designs in end-systems. Fields of research of the current year extend across 5G communications, Biotechnology, Artificial Intelligence, Internet of Things (IoT), and power-saving technologies. In an effort to keep up with the technology trends, Massachusetts Institute of Technology (MIT) and National University of Singapore (NUS) have integrated research efforts in the application of IoT and energy conservation measures to data and hardware security. Through the substantiation of theories and research projects in class, TSMC and universities are actively joining hands to cultivate new innovative semiconductor talents.

Through the substantiation of theories and research results in 2019, a total of 27 papers were published in the IEEE Journal of Solid-State Circuits (JSSC) and presented at the International Solid-State Circuits Conference (ISSCC), a prestigious conference known as the "Olympics of IC design." The number of papers published has doubled from the previous year. In addition, the research projects with University of California, Los Angeles (UCLA) and MIT have obtained the U.S. patents.

Dr. M.C. Frank Chang
Distinguished Professor of Electrical Engineering, UCLA

I appreciate TSMC’s effort in assisting National Chiao Tung University in substantializing our innovation R&D projects in high-speed fiber-optic communication, 5G communication system and AI IC through the University Shuttle Program. We are also able to verify the performance of our research results and publish them in prestigious international journals and conferences where our research efforts were received recognition.

Dr. Shyh-Jye Jou
Professor of Electronic Engineering, Institute of Electronics, National Chiao Tung University

Mixed Signal Circuit and RF Technology Application
Dr. Shen-Iuan Liu
Distinguished Professor of Electrical Engineering, National Taiwan University

Wireless Technology and Artificial Intelligence Application
Dr. Shyh-Jye Jou
Professor of Electronic Engineering, Institute of Electronics, National Chiao Tung University

Wireless Technology (5G+ and 6G) and Biomedical Sensors for Cancer Tumor Detection
Dr. Ali M. Niknejad
Professor of Electrical Engineering and Computer Sciences, UC Berkeley / Faculty Director of the Berkeley Wireless Research Center (BWRC)
Product Quality

Strategies & 2030 Goals | 2019 Achievements | 2020 Targets
--- | --- | ---
**Quality Culture Enhancement**
Promote continuous improvement programs to enhance the internal quality culture
Encourage local suppliers to participate in the Taiwan Continuous Improvement Award to strengthen a culture of quality and competitiveness within TSMC’s local supply chain

- Generate up to NT$20 billion in value from improvement projects and involve outstanding projects in the Taiwan Continuous Improvement Award
- Completed 49,356 improvement projects
- Note 2: ``Continuous Improvement Team (CIT) Activities`` and ``Suggestion Program`` have been merged into ``Improvement Projects`` in 2019

- Encourage 100% of major local raw materials suppliers and 75% of back-end packaging materials suppliers to participate in the Taiwan Continuous Improvement Award; 60% to advance to the finals
- Note 1: Major suppliers are those that meet at least one of the following conditions: 1. accounted for 85% of purchasing expenses; 2. single-source supplier; 3. ongoing orders in each quarter

**Quality Capability Improvement**
Leverage machine learning to construct a visual defect inspection and classification system for outgoing 12-inch wafers to increase employee productivity
Develop hazardous substance analysis capabilities in chemical laboratories to ensure occupational health and safety (OHS)
Strengthen management for hazardous substances to improve green manufacturing

- Increase the productivity of each visual inspection worker that are responsible for outgoing 12-inch wafers by 7,000 pieces
- Increased the productivity of each 12-inch wafer outgoing visual inspector to 5,258 pieces per month
- Note 1: Major suppliers are those that meet at least one of the following conditions: 1. accounted for 85% of purchasing expenses; 2. single-source supplier; 3. ongoing orders in each quarter

- Increase the productivity of each visual inspection worker that are responsible for outgoing packages by 5% per month and 50% accumulatively (base year: 2019)
- Developed the ability to analyze 83% of CMR substances
- Target: 77%

- Increase the productivity of each visual inspection worker that are responsible for outgoing 12-inch wafers to 5,415 pieces per month and the monthly productivity of each visual inspection worker that are responsible for back-end packaging by 5%
- Note 2: ``Continuous Improvement Team (CIT) Activities`` and ``Suggestion Program`` have been merged into ``Improvement Projects`` in 2019

- Develop the ability to analyze 100% of CMR (Carcinogenic, Mutagenic and Reprotoxic) substances and help major suppliers develop the same capabilities
- Developed the ability to analyze 83% of CMR substances
- Target: 77%

- Develop the full ability to analyze 100% of CMR substances
- Develop the ability to analyze 100% of CMR (Carcinogenic, Mutagenic and Reprotoxic) substances and help major suppliers develop the same capabilities
- NEW

- Note 2: ``Continuous Improvement Team (CIT) Activities`` and ``Suggestion Program`` have been merged into ``Improvement Projects`` in 2019
Quality Capability Improvement
Leverage machine learning to construct a visual defect inspection and classification system for outgoing 12-inch wafers to increase employee productivity. Develop hazardous substance analysis capabilities in chemical laboratories to ensure occupational health and safety (OHS). Strengthen management for hazardous substances to improve green manufacturing.

- N-methylpyrrolidone (NMP) 100% replacement (Base year: 2016)
- No process involves Perfluoroalkyl Substances (PFASs) that have more than 4 carbons

<table>
<thead>
<tr>
<th>2019 Achievements</th>
<th>2020 Targets</th>
</tr>
</thead>
<tbody>
<tr>
<td>100% compliance with hazardous substance regulations and customer requirements</td>
<td>Reduce the use of NMP by 95%</td>
</tr>
<tr>
<td>Target: 100%</td>
<td>Do not use PFASs with more than 4 carbons for the development of advanced processes of 3nm and below</td>
</tr>
<tr>
<td>86% completion of substituting all PFOA-related (Perfluorooctanoic Acid, PFOA) substances Note</td>
<td></td>
</tr>
<tr>
<td>Target: 100%</td>
<td></td>
</tr>
<tr>
<td>38% reduction in the use of NMP Note</td>
<td></td>
</tr>
<tr>
<td>Target: 70%</td>
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</tr>
</tbody>
</table>

Note: Formula and process parameter adjustments and more testing were necessary because of issues with product yield during the testing of substitute chemicals in 2019, which is why the substitution project was behind schedule.

Quality Application Realization
Based on the Company's technology roadmap, complete reliability qualification for advanced process technologies, specialty process technologies and wafer-level package process in the design and development stage.

- Complete reliability qualification for 5nm process technology, 22nm embedded MRAM and the fourth generation integrated Fan-Out packaging (InFO)

<table>
<thead>
<tr>
<th>2019 Achievements</th>
<th>2020 Targets</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Complete reliability qualification for advanced process technologies, specialty process technologies, and wafer-level package process in accordance with the R&amp;D targets</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Complete reliability qualification for 5nm process technology and specialty technologies</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Exceeded</th>
<th>Achieved</th>
<th>Missed Target</th>
</tr>
</thead>
</table>
TSMC strives to provide global customers with outstanding semiconductor foundry services. To ensure customer satisfaction, TSMC pays attention to the quality of each operational aspect and reinforces a corporate culture of consistent hard work. In face of problems and challenges, the Company stays proactive and takes effective measures to ensure that customers receive products and services of the best quality.

TSMC is leading the way for the continued advancement of semiconductor manufacturing processes and also actively trying to improve chip product quality and reliability. To fulfill its commitment to customer’s product quality and increase end user’s life quality, TSMC rigorously strives to help customers realize their product energy efficiency and high performance and achieve the goal of sustainable development. TSMC has built an IATF 16949 quality management system in line with automotive industry quality standards. The Company has leveraged information technology to build a rigorous management and quality control systems for the processes of design service, technology development, mask making, wafer manufacturing, and backend service.

Besides seeking constant improvement, TSMC also extends the quality requirements to Tier 1 and Tier 2 suppliers. Using its own experience, the Company also attempts to help partners improve their quality culture, capabilities and applications in order to enhance the quality management of TSMC, and the semiconductor supply chain.

### TSMC Quality Management System

**Design Service**
- IP/Library Development Quality Assurance
- Design Kits Deliverables Management

**Tech Development**
- SMAC Model Management
- Process Technology Development Management
- Build In Reliability Test
- Process Release Standard

**Mask Making**
- Remote Mask DB Check
- iTapeOut
- eJobView
- Mask Defect Inspection

**Wafer Manufacturing**
- Incoming Quality Control
- Advanced Process Control
- EQ Real Time Monitor
- Process Reliability Monitor
- Wafer Acceptance Test
- Outgoing Quality Gating

**Backend Service**
- Process Quality Control
- Package Reliability Monitor
- Outgoing Quality Gating

**Customer Satisfaction**
- Customer Claim Management
- Annual Customer Satisfaction Survey

**Potential Failure Mode & Effect Analysis**
- Control Plan
- Statistical Process Control
- Measurement System Analysis
- Continuous Improvement – 8Ds

**Quality Tools Application**
- Change Control Platform
- Failure Analysis
- Supplier/Subcontractor Quality Management

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**Notes:**
1. Add quality inspections for incoming materials at critical control points to ensure quality
2. Improve the real-time monitor system of photo process and establish the guideline for monitoring parameters to improve abnormal events handling flow in case of the production and delivery of defected products
3. Establish the Early Failure Rate System for real-time information in order to reduce the defect yield and risk in reliability as well as increase product yield
4. In compliance with the international standard for automotive industry, the latest version of AIAG-VDA FMEA was introduced in 2019 and is expected to be completed in 2020
5. Strengthen the connection of review between the change in mask making information and wafer manufacturing to reduce the risk of errors in the change
6. Suppliers are required to apply statistical process control and maintain the reliability of the process and the quality of upstream raw materials to enhance the analysis of such materials. The supply chain is required to receive ISO 9001 certification and to assess the management of process change in order to enhance the quality management of raw materials
Quality Culture Enhancement

Quality is the collective responsibility of all TSMC employees. In order to strengthen company’s quality culture, improve employees’ problem-solving abilities, and develop quality control systems, TSMC and its Quality and Reliability Organization held the Total Quality Excellence & Innovation Conference and series of seminars/training sessions about the design of experiments, statistical process control, metrology, and deep/machine learning in 2019. TSMC consistently encouraged its employees to innovate and drive cross-team observation and learning, and promoted the quality culture with quality awareness posters, demonstration of outstanding projects, cash bonuses, and public recognition. In 2019, employees proposed 49,300 improvement projects and generated a benefit of NT$15 billion in value. To promote employees’ initiatives as well as to prevent quality abnormalities and outdated operational regulations, the concept of "STOP & FIX" was proposed in 2019 and has created a potential benefit of NT$2.8 billion in value with over 5,500 projects, enhancing the company culture of good quality.

In 2020, TSMC continues to help employees develop quality management capabilities through the promotion and implementation of new strategies. The Company also continues to participate in the Taiwan Continuous Improvement Competition to promote outstanding projects in the local semiconductor supply chain as well as other industries in order to increase industrial competitiveness in Taiwan.

### Value of Improvement Projects

<table>
<thead>
<tr>
<th>Year</th>
<th>Target Benefit</th>
<th>Actual Benefit Created</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>110</td>
<td>100</td>
</tr>
<tr>
<td>2016</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2017</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2018</td>
<td>100</td>
<td>100</td>
</tr>
<tr>
<td>2019</td>
<td>150</td>
<td>150</td>
</tr>
</tbody>
</table>

### Categories of Improvement Projects in 2019

- **STOP & FIX**
  - Quality Improvement
    - Significantly improved cleanliness of the sputter chamber by redesigning a rougher surface texture for the chamber
    - Reduced AlPad related defects by 88%
    - Fixed etching stop layer Cu pits and hillock defect problem to reduce 5G mobile chip leakage
    - Improved 5G product yield by 40% and announced five U.S. patents
  - STOP & FIX
    - Found problems before products were scrapped and prevented the loss of NT$60 million worth of wafers

### 2019 Quality Improvement Projects

<table>
<thead>
<tr>
<th>Group</th>
<th>Projects</th>
<th>Benefit</th>
</tr>
</thead>
</table>
| Quality Improvement | Reduced charging remains on the wafer surface by improving etching de-scum capabilities | • Increased average product yield in advanced manufacturing processes by 15%
• Increased competitiveness in advanced manufacturing process and achieve customers’ AI/high-performance chip applications |
| | Significantly improved cleanliness of the sputter chamber by redesigning a rougher surface texture for the chamber | • Reduced AlPad related defects by 88% |
| | Fixed etching stop layer Cu pits and hillock defect problem to reduce 5G mobile chip leakage | • Improved 5G product yield by 40% and announced five U.S. patents |
| STOP & FIX | STOP: Avoid yield loss of new products caused by die cracks when entering volume production | • Found problems before products were scrapped and prevented the loss of NT$60 million worth of wafers |
| | FIX: Completely prevent die cracks caused by stress on ejector pins | • Found problems before products were scrapped and prevented the loss of NT$60 million worth of wafers |
Case Study

Prevent Yield Loss in New Products with STOP & FIX

TSMC has been working hard to raise quality awareness on STOP & FIX since 2019. Through promotional posters, educational training and the demonstration of outstanding projects, the Company continues to improve the corporate culture of “proactively detecting and correcting abnormalities” and to encourage employees to find potential quality risks at work and to further achieve the ultimate goal of preventing abnormalities.

In 2019, the Advanced Packaging Operations Division discovered quality abnormalities in the die of a new product. Investigations show that the problem was caused by the array of ejector pins. Therefore, the Company proposed “The Project of Improving the Array of Ejector Pins to Improve Die Yield,” to formulate the best model of stress and specification based on mechanics, and sends feedback to the R&D team to start the volume production of high-quality products. The project (1) discovers new abnormalities and develops systems of testing and prevention, and (2) improves treatment procedures and increases effectiveness and timeliness. The project also won the first place among all outstanding STOP & FIX projects in the Total Quality Excellence & Innovation Conference.

Through cause analysis and testing, the Advanced Packaging Operations Division confirmed that the array of equipment ejector pins is in the same direction as the lattice in silicon wafers so that the residual stress caused cracks in products. The best configuration of ejector pins was found through stress simulation. Continuous testing ensured that no more cracks were in the products, and the results were sent back to R&D team for the better management from original source. Around NT$ 60 million wafers were protected from being scrapped in the stage of volume production.

In the die adhesive manufacturing process of new products in the Advanced Packaging Operations Division, two consecutive die seemed abnormal in a vacuum. In addition to stopping the equipment for inspection, proactively examine the products and detect fine cracks that were considered the main cause of vacuum abnormalities. Immediately conducted the comprehensive testing and completely ceased production for the model.

Detection and Correction of Abnormalities (STOP)

In the die adhesive manufacturing process of new products in the Advanced Packaging Operations Division, two consecutive die seemed abnormal in a vacuum. In addition to stopping the equipment for inspection, proactively examine the products and detect fine cracks that were considered the main cause of vacuum abnormalities. Immediately conducted the comprehensive testing and completely ceased production for the model.

Analysis of Causes & Prevention (FIX)

Through cause analysis and testing, the Advanced Packaging Operations Division confirmed that the array of equipment ejector pins is in the same direction as the lattice in silicon wafers so that the residual stress caused cracks in products. The best configuration of ejector pins was found through stress simulation. Continuous testing ensured that no more cracks were in the products, and the results were sent back to R&D team for the better management from original source. Around NT$ 60 million wafers were protected from being scrapped in the stage of volume production.

New configuration of ejector pins is included in the development of new products to enhance product quality

<table>
<thead>
<tr>
<th>ALARM</th>
<th>Abnormalities in equipment vacuum</th>
<th>Examine the die (cracks found)</th>
<th>STOP</th>
<th>Back to equipment production</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Inspections of equipment and fab system</td>
<td>Stop the production and trace the products</td>
<td>FIX</td>
<td>Crack rate: Around 4,000 ppm → 0ppm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Find the cause (wrong position of ejector pins)</td>
<td>Prevention (New configuration of ejector pins sent to R&amp;D team)</td>
<td>Prevent wafers worth around NT$60 million from being scrapped in the stage of volume production</td>
</tr>
</tbody>
</table>

Before Improvement

After Improvement
In 2019, TSMC participated in the Taiwan Continuous Improvement Award and achieved six Gold Awards, one Silver Award, and two Best Improvement and Innovation Awards for outstanding performance. TSMC has received more Gold Awards than any other companies in Taiwan for the ten consecutive years and more Best Improvement and Innovation Awards for four consecutive years. TSMC, having won one Best Improvement and Innovation Awards each year, later showed great improvement by winning two awards for two consecutive years.

### TSMC Achievements in the Taiwan Continuous Improvement Competition

<table>
<thead>
<tr>
<th>Year</th>
<th>Gold Award</th>
<th>Silver Award</th>
<th>Bronze Award</th>
<th>Best Improvement and Innovation Award</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>5</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2016</td>
<td>4</td>
<td>2</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2017</td>
<td>6</td>
<td>2</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>2018</td>
<td>4</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>2019</td>
<td>6</td>
<td>1</td>
<td>0</td>
<td>2</td>
</tr>
</tbody>
</table>

### TSMC Projects in the 2019 Taiwan Continuous Improvement Competition

**Advancement of CMP**
- Production capacity in special technologies: 75% increase
- Bubble defect improved: 34.3%
- Total benefit: NT$512 million

**Improvement in etching defect**
- Defects decreased: 55%
- Number of scraps decreased: 78%
- Total benefit: NT$162 million

**Studying equipment’s productivity to make a breakthrough in capacity**
- Capacity of 12-inch equipment increased: 13.1%
- Productivity of employees increased: 3%
- Total benefit: NT$12 billion

**Development of new infrastructure of smart monitoring to increase the productivity of inspectors**
- Productivity increased: 51%
- Monitored amount reduced: 10%
- Monitoring speed increased: 6%
- Total number of controlled wafers and related costs reduced: 27%
- Total benefit: NT$216 million

**Advancement of Product Delivery Efficiency**
- Time spent on sending the product into the machine has been reduced by 40%
- The machine idle time for advanced process has been reduced by 3.2%
- Total benefit: NT$326 million

**Improved 3D IC Advanced Packaging Technologies**
- Annual use of chemical solutions of scrapping due to human error reduced: 14.6 kL
- Fully automated: 100%
- Total benefit: NT$183 million
As the world’s largest dedicated semiconductor foundry, TSMC always tries hard to influence and encourage local suppliers to participate in the Taiwan Continuous Improvement ward in order to improve quality management through practical achievements and increase the competitiveness of Taiwan local industry and supply chain.

In 2019, TSMC encouraged all of its major local suppliers to participate in the competition, winning three Gold Awards, six Silver Awards, four Bronze Awards, and one Best Improvement and Innovation Award in a feat that outshined performances and number of participants in 2018. In order to continuously increase the quality of its supply chain, TSMC not only invited senior management of the suppliers to attend to Taiwan Continuous Improvement Award but also required those who didn’t advance to the final to submit improvement reports. The Company published the winners’ information on the official TSMC website for public recognition, encouraging more local suppliers to make further improvements.

### TSMC Supplier Participation in the Taiwan Continuous Improvement Competition

<table>
<thead>
<tr>
<th>Year</th>
<th>Gold Award</th>
<th>Silver Award</th>
<th>Bronze Award</th>
<th>Best Improvement and Innovation Award</th>
<th>Participation Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2016</td>
<td>4</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>43%</td>
</tr>
<tr>
<td>2017</td>
<td>4</td>
<td>4</td>
<td>6</td>
<td>100%</td>
<td>74%</td>
</tr>
<tr>
<td>2018</td>
<td>1</td>
<td>4</td>
<td>4</td>
<td>100%</td>
<td>80%</td>
</tr>
<tr>
<td>2019</td>
<td>3</td>
<td>6</td>
<td>4</td>
<td>100%</td>
<td>100%</td>
</tr>
</tbody>
</table>

### Outgoing Visual Inspector Productivity for 12-inch Wafers

<table>
<thead>
<tr>
<th>Year</th>
<th>Actual</th>
<th>Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>4,247</td>
<td>4,500</td>
</tr>
<tr>
<td>2016</td>
<td>4,441</td>
<td>4,860</td>
</tr>
<tr>
<td>2017</td>
<td>4,747</td>
<td>5,250</td>
</tr>
<tr>
<td>2018</td>
<td>4,928</td>
<td>5,250</td>
</tr>
<tr>
<td>2019</td>
<td>5,258</td>
<td>5,250</td>
</tr>
</tbody>
</table>

### Detectable CMR Substances

<table>
<thead>
<tr>
<th>Year</th>
<th>Actual</th>
<th>Goal</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>2%</td>
<td>34%</td>
</tr>
<tr>
<td>2016</td>
<td>16%</td>
<td>49%</td>
</tr>
<tr>
<td>2017</td>
<td>37%</td>
<td>77%</td>
</tr>
<tr>
<td>2018</td>
<td>62%</td>
<td>83%</td>
</tr>
<tr>
<td>2019</td>
<td>83%</td>
<td>83%</td>
</tr>
</tbody>
</table>

**Quality Capability Improvement**

In order to improve quality and efficiency, in 2014, TSMC started to utilize machine learning technology and deep learning method, and successfully applied advanced spectrum analysis to automated classification of wafer defects so that differences among processes and equipment were detected, immediately triggering improvement. A defect inspection and classification system for 12-inch wafers was established to refine the consistency of outgoing inspection. In 2019, the productivity of each 12-inch wafer outgoing visual inspector has increased to 5,258 pieces per month.

The Company’s Quality and Reliability Organization, in collaboration with its Corporate ESH Division, has classified the current suspect materials and established a sampling plan for testing. As for the control and management of new materials, TSMC not only requires...
the suppliers to declare whether the provided materials comply with the regulations but also carry out sampling tests to ensure that supplier declarations are accurate. In 2019, TSMC further strengthened the ability of its chemical laboratories to analyze suspicious substance, having analyzed 83% of the substances for CMR effects. The Company also introduced testing strategies to the major suppliers, which can quickly detect 178 hazardous substances in semiconductor materials, improving their abilities to manage hazardous substances.

Better Management of Incoming Raw Materials

Before Improvement

- Incoming materials
- Important quality items inspection
- Passed
- Failed
- Require suppliers to make improvements
- Use in production

After Improvement

- Raw material specification being strictly controlled
- Incoming materials
- • Set up 100% inspection ability to quality items
- • Increase inspection sampling rate
- Certification before use
- Passed
- Passed
- Require suppliers to make improvements
- Use in production

TSMC’s Commitment to Hazardous Substance Management

- 100% compliance with law and regulations and customer standards on hazardous-substance-free products
- None additional Group 1 carcinogens as defined by the International Agency for Research on Cancer (IARC)
- Initiate early projects of the manufacturing process change and the substitution of chemicals ahead of regulatory requirements and make plans for annual replacements
- Restrict the use of long-chain PFASs with 8 carbons and above. New chemicals shall not contain short-chain PFASs with 5 to 7 carbons
In 2020, TSMC will continue to promote innovations, including smart copying the productivity and experience of 12-inch wafer outgoing visual inspectors, and setting goals of increasing the productivity of outgoing visual inspectors for back-end packaging by 5% each year.

In 2019, a batch of photo-resistor provided by a chemical supplier contained different materials that consequently caused heteropolymers in the liquid photo-resistor and had a negative effect in the 12nm and 16nm wafers produced by TSMC Fab 14B. In order to guarantee wafer quality, TSMC immediately scrapped the defective wafers, informed all impacted customers, proposed alternative plans through individual communication, and strengthened online wafer testing to enforce stronger controls on incoming materials. In addition, TSMC increased capabilities of testing incoming materials provided by suppliers and enforced a certification procedure before using the materials in production in order to ensure that the quality is in accordance with requirements of the advanced process technology.

In 2019, TSMC, in collaboration with SEMI, invited SEMICON, which had only been held in the U.S. and Europe, to hold the forum in Taiwan for the first time in order to increase the competitiveness of Taiwan local supply chain in the global semiconductor industry. 55 suppliers and 147 industry representatives participated in the event. TSMC also shared its innovations and management regarding the analysis of CMR substances as the Company has been dedicated to helping the global semiconductor industry produce higher-quality green products and realizing the goal of global sustainable management.

Regarding the chemical management in manufacturing process, TSMC considers the comprehensive management of hazardous substances an important step in improving quality capability. The replacement plan of PFOA-related substances continued in 2019. Photo-resistor, the chemical that contains PFOA, is a key material in the manufacturing process. TSMC has tested a new, PFOA-free photo-resistor multiple times but problems with product yield means that formula and processing parameters must be adjusted and therefore delaying the substitution project. By May 2020, the completion rate has reached 86%. It is expected to reach 100% by the end of 2020. As for short-chain PFASs with 4 carbons, which has received worldwide attention, TSMC started an investigating/evaluating substitution project regarding existing chemicals in 2019 and also conducted evaluations of excluding such substances in the R&D phase.

In addition, TSMC has initiated a replacement project ahead of regulatory requirements regarding NMP, a commonly used chemical recognized as toxic for birth and reproduction. In 2019, the NMP substitution project also faced issues with product yield because of substituting chemicals. TSMC will continue to make formula adjustments and more testing to reach the goal of reducing the use of NMP by 95% in 2020.

For more details, please refer to TSMC CSR website: TSMC Collaborates with SEMI to Hold the Strategic Materials Conference in Taiwan for the First Time.
Quality Application Realization

TSMC’s Quality and Reliability Organization is in close collaboration with its R&D team, and continues to focus on the advanced logic manufacturing process, specialty process, advanced packing technologies development and quality qualification to ensure that component features, product yield and reliability meet the requirements.

As for the advanced logic manufacturing process, in 2019, TSMC completed the qualification for 5nm FinFET transistors to ensure that its 5nm process technology is highly competitive for mobile communication and high-performance computing applications. The 5nm process is expected to enter volume production in 2020. In the aspect of specialty process technologies, qualification for embedded Magnetic Random Access Memory (MRAM) on TSMC 22nm Ultra-Low Leakage (22ULL) process platform has been completed. As for CMOS image sensor technology, TSMC has completed the qualification for 45nm near infrared CMOS (Complementary Metal Oxide Semiconductor) image sensor and ASIC (application-specific integrated circuits) Wafer-on-Wafer application.

In order to continue reducing product defects, improve process control, detect abnormality early on, and prevent quality incidents from affecting customers, TSMC’s Quality and Reliability Organization and Fab Operation are collaborating in a cross-team effort to apply advanced statistical techniques and quality tools towards the creation of an immediate defense system in wafer factories. In 2019, TSMC continues to enhance the design and application of automotive products and update the automotive quality system to version 2.0. The Company also provided exclusive resources to its customers in the automotive industry with DPPM demands so they can conduct analysis on returned merchandise and real-time Physical Failure Analysis (PFA) to drive process improvement. In 2019, TSMC established the quality control of automotive products on its 7nm and 12nm process technologies so that the Company is ready for the automotive electronics market in 2020.

TSMC did not have any massive product recall in 2019, showing that TSMC products have been able to reach or exceed customers’ demand for quality and reliability. With manufacturing excellence and high-quality service, TSMC will support customers to seize the business opportunities in the four growing markets that are mobile communication, high performance computing, IoT (Internet of Things) and automobile electronics, increase their competitiveness, provide global consumers high-quality electric products, and bring everyone a better life.

For more details of Product Quality, please refer to TSMC’s 2019 Annual Report.
## Customer Service

<table>
<thead>
<tr>
<th>Strategies &amp; 2030 Goals</th>
<th>2019 Achievements</th>
<th>2020 Targets</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Precise Response</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| Provide excellent customer service through close collaboration with customers and customer meetings/surveys on a regular basis to understand and respond to their needs | Customer satisfaction rating of 93%  
Target: >90% | Maintain customer satisfaction rating of over 90%  
Every million 12-inch wafers shipped, improve the number of engineering quality or reliability issues to 95% of the level in 2019 |
| Maintain customer satisfaction rating of over 90% |                   |              |
| Every million 12-inch wafers shipped, the number of engineering quality and reliability issues improved to 60% of the level in 2019 |                   |              |
| **Virtual Fab**        |                   |              |
| Provide comprehensive information in a timely manner to ensure the success of customer’s products; strengthen processes and systems to hold the highest stands to protect customer product information | In line with TSMC’s technology roadmap, provided customers with over 765 types of available wafer manufacturing and process technology  
Passed customer product information audit with no major flaws  
Target: No major flaws. | Provide customers with over 800 types of available wafer manufacturing and processing technology; over 60 types of advanced packaging technology  
Pass customer product information audit with no major flaws  
Target: No major flaws. |
To become customers’ trusted partner, TSMC vigorously strives to provide the best service to customers as to help customers achieve success. TSMC has established a devoted customer service team, which is a dedicated coordination window to provide the timely assistance and creates the best customer experience, from design support, mask making, and wafer manufacturing, to backend services. TSMC also commits to protect customer’s confidential information with highest standard. TSMC wins customer’s continuous trust, and was chosen as their foundry service provider, thereby ensuring TSMC’s continue growth in the future.

Precise Responses

TSMC treats customer feedback and expectations as an important basis for improving and developing customer relationship. TSMC learns about customer needs through multiple channels, and customers can then utilize these channels to provide feedback on the performance of business behavior, relationship, technology, quality, yield, design support, manufacturing, customer service, and further expectations for the future. TSMC reviews and analyzes customer feedback regularly, develop improvement plans upon them, and view it as a complete customer needs handling process. According to the annual customer satisfaction survey in 2019, TSMC received a high score of 93%, keep maintaining high rating above 90% in 6 consecutive years. In 2019, in response to customers’ expectation in continuous quality improvement for product segments required higher quality, TSMC created a new theme of improvement: “STOP & FIX.” Combining with a series of quality training activities, TSMC strengthens employees’ capability to provide quality services and encourages employees to adhere to the quality and be the front-line guardian of quality. In an ever-changing market, the close collaboration with customers helps TSMC continuously satisfy its customers’ needs with advanced technology, manufacturing excellence, and high-quality service.

The Customer Service Strategy Pyramid

Various Communication Channels for Customers

Annual Customer Satisfaction Ratings

<table>
<thead>
<tr>
<th>Year</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>93</td>
</tr>
<tr>
<td>2016</td>
<td>95</td>
</tr>
<tr>
<td>2017</td>
<td>93</td>
</tr>
<tr>
<td>2018</td>
<td>93</td>
</tr>
<tr>
<td>2019</td>
<td>93</td>
</tr>
</tbody>
</table>

Note: Index includes Taiwan Facilities and Subsidiaries
collaboration provides information about customer analysis, as well as quality and reliability data. Logistics engineering, lots, wafer yields and wafer acceptance test of design life cycle. Engineering collaboration provides accurate and the most updated information at each stage. Customers thus play an active role in collaborations with its customers in design, engineering and logistics. Customers thus have a 24-7 access to critical information and are able to create customized reports to facilitate effective wafer management. Design collaboration provides information about customer order placement, shipments and delivery. To serve as a customer’s “virtual fab,” through TSMC-Online<sup>TM</sup>, customers can access transparent and comprehensive wafer manufacturing information and services. Thereby, customers can manage their products on a real-time basis to achieve product success. In 2019, in line with technology roadmap, TSMC now provides customers with over 780 types of available wafer manufacturing and process technologies and over 60 types of advanced package technologies. Proprietary Information Protection is a promise from TSMC to guarantee the interests of its customers. As a customer’s “virtual fab,” TSMC holds the highest standard to protect its customers by implementing a special safety monitoring mechanism throughout the whole production process with annual audit of all control points.

In 2019, TSMC helped customers achieve ISO 15408 certification for various types of high-security chip products. ISO 15408 certification, an international standard under the Common Criteria for Information Technology Security Evaluation, is a security evaluation standard for information products and systems. It is given in two major forms: product certification and site certification. To avoid any redundancy certification process on the part of its customers and provide a better customer experience by expediting customer’s product certification processes, TSMC continues to obtain site certifications for its various foundry businesses according to demands. In 2019, TSMC successfully achieved ISO 15408 certification for its Fab 14B. Compliant to the highest standard for the production of security products and the protection of proprietary information, Fab 14B is fully qualified to readily accept orders for high-security products. For customers with such demand, therefore, TSMC is able to provide a safe manufacturing environment and ensure optimal safety management not only in the production process but also along the supply chain. Furthermore, TSMC ensures the safety and reliability of the end-products manufactured with its security and aims to pass all annual inspections on customer products and information protection, thereby deepening trust and partnership with its customers.

TSMC strongly believes that constant innovation and high-quality products and services are the key factors to maintain a long-lasting customer satisfaction. As a trusted technology and capacity provider in the global logic IC industry, TSMC will continue to be service-oriented and maximum-total-benefits silicon foundry as to become a long-term important partner that customers can trust and rely on for success.

### Types of Wafer Manufacturing Technology/Advanced Packaging Technology

<table>
<thead>
<tr>
<th>Years</th>
<th>Types of Wafer Manufacturing Technology</th>
<th>Types of Advanced Packaging Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>2015</td>
<td>510</td>
<td>10</td>
</tr>
<tr>
<td>2016</td>
<td>575</td>
<td>22</td>
</tr>
<tr>
<td>2017</td>
<td>628</td>
<td>31</td>
</tr>
<tr>
<td>2018</td>
<td>701</td>
<td>46</td>
</tr>
<tr>
<td>2019</td>
<td>765</td>
<td>60</td>
</tr>
</tbody>
</table>

Note 1: 2019 index includes Taiwan Facilities and Subsidiaries.
Note 2: The cut-off date of “types of wafer manufacturing technology” and “types of Advanced Packaging Technology” is December 31.
**Case Study**

**Enhance Self-Service Wafer Instructions - Real Time Customer Service**

In 2019, to improve the timeliness and convenience of customers wafer manufacturing instruction, TSMC integrated product information and wafer production system, improved customer lot handling notice process, and enhanced TSMC-Online™ function. Now, customer can release manufacturing instructions to not-yet processed wafer or stacked-wafer products in TSMC-Online™ without time-zone constraint. Before this enhancement, if customer had manufacturing instruction to not-yet processed wafer or stacked-wafer product which is with complicate manufacturing process, customer need to contact TSMC off-line. Then TSMC counterpart would help to release customer’s instruction accordingly. Now, customer can per request to reserve wafer ID with manufacturing instruction in TSMC-Online™. The instruction will be released to manufacturing system directly after confirmation. Besides, TSMC integrated the information from Bill of Material and wafer production system. Combining with optimized system user interface, customers have a clear overview of wafer status and wafer instruction process in TSMC-Online™. This new service enhancement can reduce wait time from time zone differences. After the new functions launched in March 2019, the usage rate increased by 22% and timeliness improved by 20%.

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**Customer request**

1. **Original process**
   - Check wafer status with TSMC
   - Discuss needs with TSMC
   - TSMC releases instruction
   - TSMC confirms

2. **Improved process**
   - Customer request
   - TSMC Online™
     - Online query wafer status
     - Online book new lot ID
     - Online release instruction
     - TSMC confirms

**TSMC Online™**

- Convenience
- 20% Timeliness
- 22% Usage Rate
Proprietary Information Protection

Proprietary Information Protection is a promise from TSMC to customers, shareholders and employees. TSMC responds to the increasing importance of proprietary information protection in regard to maintaining current and future competitive advantage, and devises "Proprietary Information Protection — PIP" policy to define the proprietary information protection and management guidelines. TSMC trade secrets and related undisclosed confidential information are protected under these guidelines in the best interest of company, shareholders, employees, customers, and vendors.

TSMC has created its PIP Committee, an organization dedicated to the Proprietary Information Protection, chaired by senior vice president of information technology and materials management & risk management. Consisting of Vice Presidents from legal counsels, Human Resource, R&D, and Operations, the committee holds regular meetings to review and develop important policies on information protection and information security. It creates and enforces Proprietary Information Protection policy and guidelines, develops effective compliance mechanism, continues to enhance its capability to protect proprietary information, and ensures the applicability of those regulations through yearly reviews. Amendments were made in 2019 to guidelines on proprietary information management and to physical security area definition. Seven major approaches were adopted to consolidate and protect Company’s proprietary information.

TSMC’s Strategy for Proprietary Information Protection

TSMC considers the Proprietary Information Protection (PIP) as part of its core business strategy. To fulfill its commitment to PIP, the Company has adopted four approaches: information classification and control, access authorization, training programs, and compliance auditing. These measures serve to protect the proprietary information of not only TSMC and its subsidiaries but also any third party entity that conducts business dealings with TSMC. Furthermore, TSMC continues to enforce IT security measures, actively identifying potential vulnerabilities and risks for data breach, assessing possible damages, and developing mitigation measures to fulfill its commitment to Proprietary Information Protection.

Seven Major Approaches of PIP Implemented in 2019

- Printed Material Management
- Employee Access Control
- Facility Management
- Information Control
- Equipment Management
- IT Asset Management
- IT System/Application Management
IT Security Management Measures in 2019

TSMC has developed specific methods for the assessment of information security risks, created clear protocols for management, built automated information security management system, and obtained ISO 27001 certification for information security, thereby becoming compliant with international standards for information security management. In response to all kinds of cyber-attacks and external threats to information security, TSMC continued in 2019 to enforce information security risk management measures, enhance detection, and strengthen defensive measures. For example, TSMC has created automated anti-virus system to prevent malware from infiltrating into its intranet; it has strengthened the control of intranet and firewalls to prevent the spread of virus across facilities or equipment; it has installed endpoint anti-virus measures; it has developed and deployed information security monitoring applications to monitor internal computers and alert of any security problems; it has stepped up detection of computer vulnerabilities and ensured that software programs are up-to-date; it has also enhanced detection of phishing emails and taught employees how to identify them. TSMC ensures the validity and legitimacy of information security protocols and procedures through regular reviews and evaluations, thereby minimizing information security risks and protecting the company from ever-evolving and ever-growing security threats.

Training and Campaigns for PIP & Information Security

TSMC offers regular and diverse training programs and conducts continued promotion programs to impose PIP awareness and obligations on all employees, making them recognize the importance of PIP and to equip them with the knowledge and capabilities needed to minimize the risk of information breach. For example, the Company has taught its employees how to identify phishing emails and provided clear guidelines to employees and contractors to avoid infractions of information security protocols. Furthermore, TSMC targets its efforts at employees by establishing internal PIP Working Committees in its organizations and functional units. In a total of 60 organizations, including TSMC’s Taiwan facilities and overseas subsidiaries, PIP Guardians hold monthly meetings to keep track of situations on the ground, raise suggestions on information security for their organizations, and design PIP measures that meet the specific needs of their organizations, keep pace with changing conditions, and adapt to local circumstances. In addition, employees can raise their PIP concerns and report information security incidents through a Helpdesk hotline or an online suggestion box. The reports will be handled and addressed by dedicated staff.

For suppliers, TSMC established Supplier’s Chain Security Association in 2019, which holds Supply chain security interaction meeting with important suppliers that work closely with the company to discuss Proprietary Information Protection and information security policies and possible improvements. To protect the interest of both parties by avoiding information breach, TSMC launched a quarterly newsletter of TSMC Supply Chain Security Newsletter from the third quarter of 2019 to keep suppliers updated about any change in regulations and the newest announcements.

Structure of Information Security Management System

| Detection | Internal and external threats to information security are regularly detected. |
| Recovery | Recovery procedures are executed to restore functions and conduct tests. |
| Response | In the event of information security incident, comprehensive response plans are executed. |
| Identification | Threats to information security are identified and analyzed to inform defensive measures. |
| Control | Factors affecting information security are pinned down to inform action plans and enforce control measures. |

PIP and Information Security Incident Reporting

- **Employees**
  - Report concerns through PIP Helpdesk/suggestion box
- **PIP Report Coordinators**
  - Identify the nature of concerns and refer them to dedicated staff
  - Address the concerns based on the impacts and the risks involved
  - Launch investigations and give penalties when infractions being identified
- **PIP Staff**
  - Provide updates on the measures taken and results to employees who raised the concern

- **Measures and Results**
Note 1: 2019 PIP performance indicators cover TSMC’s Taiwan facilities, TSMC (China), and TSMC (Nanjing).

Note 2: To strengthen the protection of proprietary information, TSMC enforced inspection and detection measures for printed documents and physical security in 2019, resulting in a higher infraction rate than the year before.

Newly created or revised 12 PIP regulations

1.29% of employees were caught violating PIP regulations and were given penalties consistent to the severity of damage caused by their violations. Penalties include demerit, warning, and suspension of duty. Major violation will result in termination of employment and lawsuit (i.e., Trade Secret Law).

The main cause of violation: personal negligence or practices not compliant to PIP protocols.

Corrective measures:
- Strengthen PIP promotion campaigns and training programs
- Reinforce control on data access and data distribution
- Reinforce control on document printing and data access
- Offer online consultancy service and training programs on new regulations

Over 48,000 employees completed the annual PIP online refresher e-learning course.

Course content:
- Core concepts that underlie PIP policies
- Major events and new regulations in 2019
- Case studies on PIP regulatory violations
- Ways to check PIP regulations and seek consultancy if needed

All new employees, a total of over 3,000 individuals, have completed PIP training courses.

All new vendors, a total of over 25,000 individuals, have completed PIP training courses.

A total of 24 PIP posters were created to promote important regulations and announcements.

A PIP Micro-film Contest was held with 14 microfilms created, in which Vice President level or above executives reminded employees the importance of PIP to TSMC’s competitive edge.

The main cause of violation: personal negligence or practices not compliant to PIP protocols.

Corrective measures:
- Strengthen PIP promotion campaigns and training programs
- Reinforce control on data access and data distribution
- Reinforce control on document printing and data access
- Offer online consultancy service and training programs on new regulations

95 Points
95 points average score for employees PIP engagement. Conducted a PIP engagement survey, collected over 40,000 surveys with over 85% response rate.

14 PIP Micro-film
A PIP Micro-film Contest was held with 14 microfilms created, in which Vice President level or above executives reminded employees the importance of PIP to TSMC’s competitive edge.

24 PIP Posters
A total of 24 PIP posters were created to promote important regulations and announcements.

48,000 Employees
Over 48,000 employees completed the annual PIP online refresher e-learning course.

Course content:
- Core concepts that underlie PIP policies
- Major events and new regulations in 2019
- Case studies on PIP regulatory violations
- Ways to check PIP regulations and seek consultancy if needed

1 Fab achieved ISO 15408 certification
Fab 14B was successfully certified by the German Federal Office for Information Security (BSI) for ISO/IEC 15408-EAL6 under Common Criteria (Site Certification), thus becoming fully qualified to readily accept orders for security chips and high-security products.

Approximately 3 million PIP checks conducted per month, including:
- PIP contraband detection
- Entry control on premises
- Inspections on the handling of proprietary information
- Inspections on the use of emails
- Inspections of contractors’ PIP practices

3 Million Checks
Number of PIP Inspections Conducted Each Month

0 Case
Zero cases of customer information breach from information security incident

2019 Proprietary Information Protection Enforcement Report

3 Million Checks
Number of PIP Inspections Conducted Each Month

2019 Customer Security Audits
TSMC assisted four customers in obtaining international security certifications for their products, and ensured their product information protection during manufacturing.

100%
All new employees, a total of over 3,000 individuals, have completed PIP training courses.

100%
All new vendors, a total of over 25,000 individuals, have completed PIP training courses.

12 Regulations
Newly created or revised 12 PIP regulations

1.29%
1.29% of employees were caught violating PIP regulations and were given penalties consistent to the severity of damage caused by their violations. Penalties include demerit, warning, and suspension of duty. Major violation will result in termination of employment and lawsuit (i.e., Trade Secret Law).

The main cause of violation: personal negligence or practices not compliant to PIP protocols.

Corrective measures:
- Strengthen PIP promotion campaigns and training programs
- Reinforce control on data access and data distribution
- Reinforce control on document printing and data access
- Offer online consultancy service and training programs on new regulations

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2017 2018 2019

3 Million Checks
Number of PIP Inspections Conducted Each Month

2017 2018 2019

95 Points
95 points average score for employees PIP engagement. Conducted a PIP engagement survey, collected over 40,000 surveys with over 85% response rate.

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TSMC Delivers Unrivalled Manufacturing Flexibility

>12 Million

The output volume in 2019 exceeded 12M in 12-inch wafer equivalents